LOWERED PU POWER USAGE METHOD AND APPARATUS

ABSTRACT OF DISCLOSURE

Disclosed is an apparatus which places computer program instructions into instruction channels in accordance with predefined criteria such that at least some external event instructions are placed in a special "blocking channel." The number of instructions, in a channel, is monitored in channel specific counters. When a computer processor is awaiting a response from an external entity event (in other words, is blocked from proceeding with the operation the PU is attempting), as signified by the blocking counter being at a predetermined value, the entire PU or at least processor auxiliary components that would be idle, such as math logic, while awaiting an external event response, are deactivated to save power until an awaited external event response is received.